Surface potential study of amorphous In–Ga–Zn–O thin film transistors

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In this paper, we report on surface potentiometry in the channel region of operating amorphous In–Ga–Zn–O thin film transistors by scanning kelvin probe microscopy. Important parameters including the field-effect mobility and source/drain contact resistance are extracted from the channel potential profile. We find that the channel potential as a function of gate/drain bias can be described by the standard metal oxide semiconductor field effect transistor (MOSFET) equation incorporated with two nonideal factors: the gate-voltage-dependent field-effect mobility and the source/drain contact resistance. © *2010 American Institute of Physics*. [doi:10.1063/1.3503871]

I. INTRODUCTION

Scanning kelvin probe microscopy (SKPM) offers the possibility to measure two-dimensional (2D) electrostatic potential distribution with high spatial resolution, and has been successfully applied to studies of many inorganic/organic semiconductor structures. Arakawa *et al.*[1] reported on 2D potential distribution of cleaved GaAs high electron mobility transistors (HEMTs), and observed a potential knee possibly originating from the trapped charge at the epitaxial layer/substrate interface. The current crowding phenomenon was also confirmed to occur at the edge of the drain electrode. Sadewasser *et al.* obtained the surface work function of chalcopyrite solar cells,[2] and observed downward band bending at the grain boundaries due to charged defect states. Recently, an extensive amount of work characterizing the surface potential of organic thin film transistors (TFTs) has been reported, investigating the charge transport mechanism,[3–5] hole density of states,[6] contact resistance,[7,8] field-effect mobility,[9] and local fluctuation of the surface potential due to inhomogeneities of the organic layer.[10,11]

So far, the potential profile of working transparent metal-oxide TFTs has not been reported. In this work we utilize SKPM to map the surface potential in the channel region of amorphous In–Ga–Zn–O (a-IGZO) TFTs with bias voltage. The provided information will be very useful for understanding the device operation principles and for designing higher performance device structures.

II. EXPERIMENTAL SETUP

Figure 1 shows our experimental setup. We use an Asylum MFP-3D system in noncontact mode to perform SKPM. The system has two feedback loops. The z feedback loop operates as an atomic force microscope (AFM), and generates surface topography images. In the voltage feedback loop, both dc and ac bias signals are applied to the cantilever. Assuming that the electrical interaction between the cantilever tip and the sample can be approximated by two parallel plates, the voltage between can be written as

$$V(t) = V_{dc} + V_{ac}\sin(\omega t) - V_{ch}, \tag{1}$$

where V_{dc} is the applied dc signal, V_{ac} and ω are the amplitude and frequency of the applied ac signal, and V_{ch} is the surface potential of the sample (TFT back channel). An expression of the electrostatic force between the tip and sample can be derived from Eq. (1)

$$\begin{aligned} F(t) &= C \times V(t)^2/d \\ &= (C/d) \times \left\{ \left[(V_{dc} - V_{ch})^2 + \frac{1}{2} \times V_{ac}^2 \right] \right. \\ &\quad + 2 \times (V_{dc} - V_{ch}) \times V_{ac}\sin(\omega t) \\ &\quad \left. - \frac{1}{2} \times V_{ac}^2 \cos(2\omega t) \right\}, \end{aligned} \tag{2}$$

where C is the capacitance, and d is the tip-to-sample spacing. The amplitude of the ac part with frequency ω is zero when $V_{dc}=V_{ch}$, that is, when the applied dc bias signal matches the surface potential. The voltage feedback loop thus varies V_{dc} to zero the ω signal, and the image created from the variation in V_{dc} is the image representing the TFT surface potential.

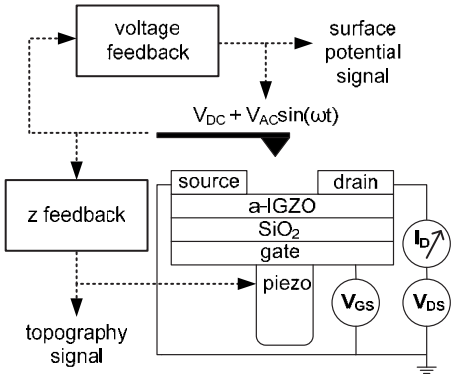

FIG. 1. Experimental setup used for a-IGZO TFT surface potential measurements.

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The MFP-3D system utilizes a dual pass technique. During the first pass, topography z(x) is obtained by the noncontact AFM mode. After completing a line, the tip is elevated 300 nm above z(x). The same line is scanned again, and the surface potential data is collected during the second pass. It has been shown for organic TFTs that if the channel is free of net space charge, then the surface potential closely follows the channel potential in the accumulation layer for TFTs based on unintentionally doped semiconductors.[3,4,9,12] We also verified through device simulations that the surface potential difference in the back channel interface (surface exposed to air) was very similar to the potential difference in the conduction channel interface for inorganic amorphous semiconductors such as amorphous silicon and a-IGZO, although some difference can be observed for very thick films (semiconductor thickness larger than 200 nm); in this experiment the a-IGZO thickness is 20 nm. We recognize that it is important to control both the back and front interface for proper and stable device operation. It is known that exposure of the back interface to plasma (of argon, nitrogen, oxygen, hydrogen, or water) can affect the a-IGZO electrical performance and stability, e.g., larger off-current and threshold voltage shift, and a large hysteresis in current–voltage characteristics can be observed. The hydrogen and nitrogen can be donor to a-IGZO. However the a-IGZO TFT electrical performance and stability are not affected by device storage in air at room temperature for several months. We have verified experimentally that the a-IGZO TFT electrical properties (including off-current, hysteresis and stability) did not changed by simple exposure of the back interface to air during storage or device operation at room temperature. We also verified experimentally that the initial (before experiment is started) and final (after experiment is completed) current-voltage characteristics were the same indicating that our assumption indicated above is valid. Of course for practical applications the top a-IGZO surface should be passivated by silicon oxide/silicon nitride double layer. For example a combination of the sputtering (silicon oxide) and plasma enhanced chemical vapor deposition (silicon nitride) can be used to realize such double layer. It is important that the first layer (which in direct contact with exposed top surface) is deposited with low hydrogen and nitrogen content. Therefore, we consider that the a-IGZO TFT back channel surface potential measured by SKPM represents the potential profile within the TFT channel interface.

The experiment was repeated several times. Only representative experimental results are shown and discussed below. In general, we did not see any variation between experiments once the experimental set-up is properly grounded.

The a-IGZO TFT used in this study has an inverted-staggered structure. A heavily-doped n-type Si wafer and thermally-oxidized SiO_2 layer (100 nm thick) serve as the gate electrode and gate dielectric, respectively. The a-IGZO active layer (20 nm) was deposited by rf magnetron sputtering at room temperature, and patterned by wet etch. Finally, an Au/Ti stacked film (40 nm/5 nm) was deposited as source/drain electrodes by electron-beam vapor deposition and patterned by lift-off.[13,14] The a-IGZO TFT (W/L $=60\ \mu m/10\ \mu m$) transfer (I_D versus V_{GS}) and output characteristics (I_D versus V_{DS}) are shown in Fig. 2. The device demonstrated good electrical properties: field-effect mobility and threshold voltage extracted by linear fit method [shown in the inset of Fig. 2(a)] yield 12 cm^2/V s and 3 V, respectively, very sharp subthreshold slope 0.15 V/dec, Off-current in the order of 10^{-12}–10^{-11} A, and current on-off ratio exceeding 10^7. The a-IGZO TFT was biased when collecting the topography and surface potential images. The gate was biased by the Asylum MFP-3D system, while the source/drain was biased externally by a Keithley 2400 SourceMeter. The drain current was also measured simultaneously by the Keithley 2400. All instruments were grounded together.

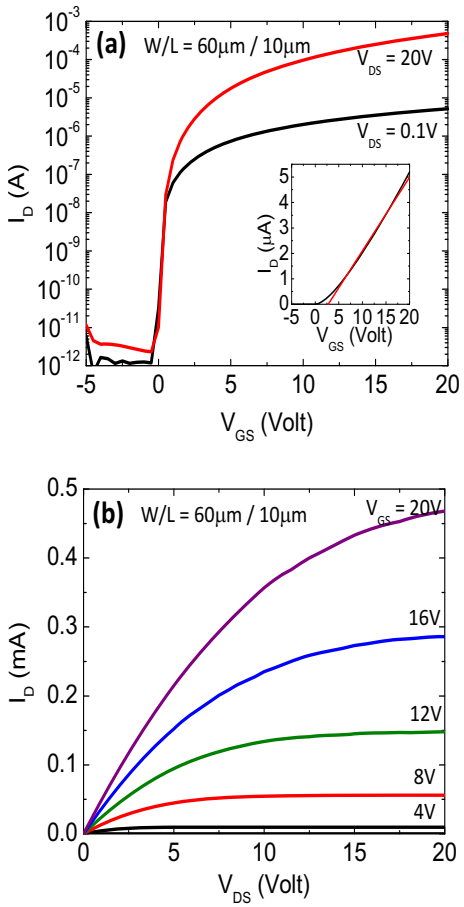

FIG. 2. (Color online) Transfer characteristics (a) and output characteristics (b) of a-IGZO TFT.

III. SURFACE POTENTIAL MEASUREMENT RESULTS

Figure 3(a) shows the a-IGZO TFT (W/L $=60\ \mu m/10\ \mu m$) channel region surface topography (z). The channel ($x=5-15\ \mu m$) between the source and drain electrodes can be clearly seen. Figure 3(b) shows the TFT potential profile (V_{ch}) obtained without bias ($V_{GS}=V_{DS}=0$ V), and serves as a base line for this experiment (this potential was subtracted from all potential profiles with bias). Figures 3(c) and 3(d) show the potential profiles obtained when $V_{DS}=5$ V while V_{GS} was increased from 1 V, 2 V, to 10 V, and $V_{GS}=5$ V while V_{DS} was increased from 1 V, 2 V, 5 V, to 10 V, respectively. A sudden rise in potential $V_{S/D}$ at the source/channel and channel/drain interfaces is observed.

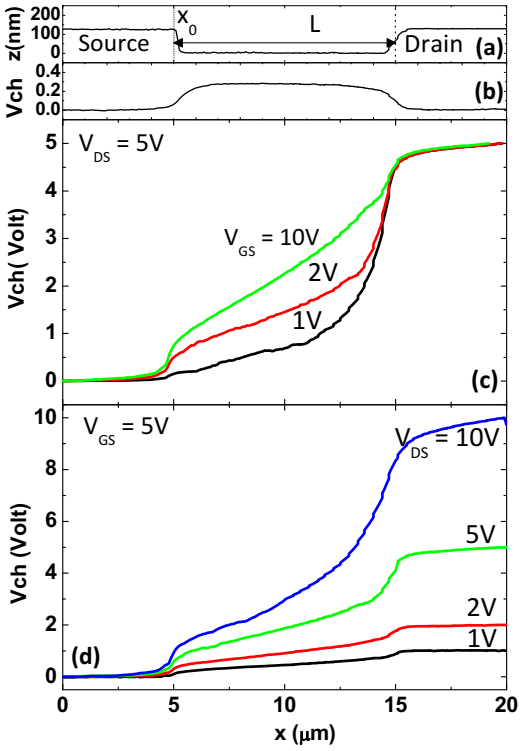

FIG. 3. (Color online) a-IGZO TFT surface topography (a), and potential profiles obtained without bias (b), and when V_{DS}=5 V while V_{GS} was increased from 1, 2, to 10 V (c), and when V_{GS}=5 V while V_{DS} was increased from 1, 2, 5, to 10 V (d).

The source/drain contact resistance $R_{S/D}=(V_S+V_D)/I_D$ is determined to be 28.6 kΩ (V_{DS}=1 V, V_{GS}=5 V, I_D=7 μA), which is consistent with the previously reported contact resistance extracted from the transmission line method ($R_{S/D}$ ~20 kΩ, V_{DS}=0.1 V, V_{GS}=5 V, W=180 μm).[15] Useful information related to the operation principle of a-IGZO TFT can also be studied based on the channel region potential profiles. In the linear regime of TFT operation, a linear increase in potential (V_{ch}) from the source to drain was observed. The potential profile becomes superlinear in the saturation regime, and rises more at the drain end than at the source end. This can be better appreciated when plotting the lateral electric field along the channel, $E_L(x)=-dV_{ch}(x)/dx$, as shown in Fig. 4. Notice that the electric field changes rapidly at the drain end for increasing values of V_{DS}. At the source end, the magnitude of the field increases with V_{DS} for small values of V_{DS} but increases at a slower rate as the TFT enters the saturation regime.

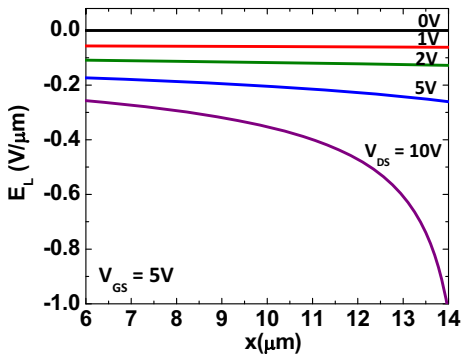

FIG. 4. (Color online) Lateral electrical field along the TFT channel.

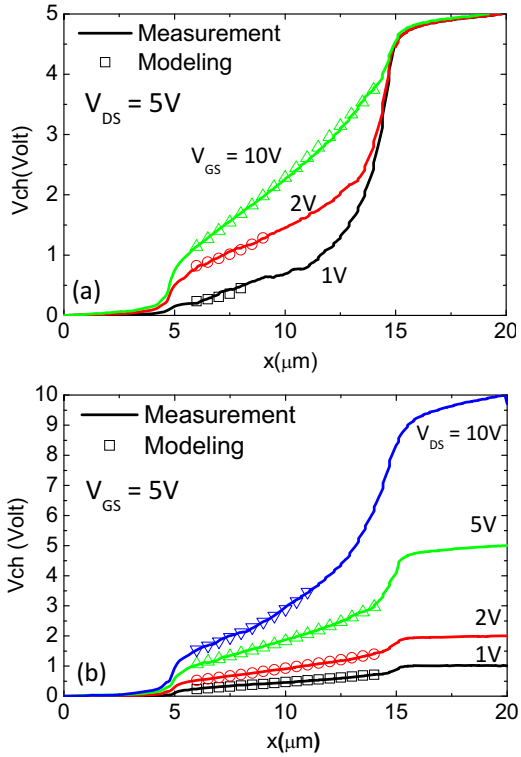

FIG. 5. (Color online) Measured (lines) and calculated (symbols) $V_{ch}(x)$.

The drain current (I_D) was also measured while collecting the surface potential images and can be described by

$$I_D = W \times \mu(x) \times Q_{ch}(x) \times E_L(x)$$

$$= W \times C_{ox} \times \mu_0 \times [V_{GS} - V_T - V_{ch}(x)]^{1+\gamma} \times \frac{dV_{ch}(x)}{dx}$$

$$\Rightarrow I_D \times dx = W \times C_{ox} \times \mu_0 \times [V_{GS} - V_T - V_{ch}(x)]^{1+\gamma} \times dV_{ch}(x), \quad (3)$$

where W is the channel width, C_{ox} is the gate capacitor per unit area, V_T is the TFT threshold voltage, $E_L(x)=-dV_{ch}(x)/dx$ is the lateral electric field along the channel, $[V_{GS}-V_T-V_{ch}(x)]=V_{ox}$ is the potential drop across the gate insulator, and $Q_{ch}(x)=-C_{ox}\times[V_{GS}-V_T-V_{ch}(x)]$ is the induced channel charge per unit area. The field-effect mobility $\mu(x)=\mu_0\times[V_{GS}-V_T-V_{ch}(x)]^{\gamma}$ is dependent on V_{ox} where μ_0 is the fitting parameter associated with the field-effect mobility and γ is the nonlinearity factor.[14–16] We can therefore find $V_{ch}(x)$ by integrating Eq. (3) from x_0 to x, where x_0 is the x position of the source/channel interface, and $V_{ch}(x_0)=V_S$ is the sudden potential rise at x_0 due to the source contact resistance R_S.

$$I_D \int_{x_0}^{x} dx = W \times C_{ox} \times \mu_0 \times \int_{V_{ch}(x_0)}^{V_{ch}(x)} (V_{GS} - V_T - V_{ch})^{1+\gamma} dV_{ch}$$

$$\Rightarrow I_D = \frac{W \times C_{ox} \times \mu_0}{(2+\gamma) \times (x - x_0)} \times \{(V_{GS} - V_T - V_S)^{2+\gamma} - [V_{GS} - V_T - V_{ch}(x)]^{2+\gamma}\}. \quad (4)$$

Solving for $V_{ch}(x)$ yields

$$V_{ch}(x) = (V_{GS} - V_T) - \left[(V_{GS} - V_T - V_S)^{2+\gamma} - \frac{(2+\gamma) \times I_D \times (x - x_0)}{W \times C_{ox} \times \mu_0} \right]^{(1/2+\gamma)}. \quad (5)$$

Figure 5 shows the calculated $V_{ch}(x)$ using $\mu_0 = 7.7\ cm^2/V^{1+\gamma}s$, $\gamma = 0.3$, $V_T \sim 0.6$ V, and $x_0 = 5$ μm. Comparable nonlinear factor values ($\gamma = 0.3-0.45$) have been reported for different a-IGZO TFT samples.[14–16] A good fit between the measured and modeled data can be seen, indicating that the standard metal oxide semiconductor field effect transistor (MOSFET) equation incorporated with the nonlinear factor and source/drain contact resistance describes very well the channel potential of a-IGZO TFTs. Please note that Eq. (5) is only valid until the "pinch off" point in the channel where $V_{ch}(x) < V_{GS} - V_T$.

The apparent current-voltage characteristics of a-IGZO TFTs which is constant along the channel (independent of x) can be obtained by integrating Eq. (3) from x_0 to (x_0+L)

$$I_D = \frac{W \times C_{ox} \times \mu_0}{(2+\gamma) \times L} \times [(V'_{GS})^{2+\gamma} - (V'_{GS} - V'_{DS})^{2+\gamma}] \quad \text{for } V'_{DS} \le V'_{GS}, \quad (6)$$

where $V'_{GS} = (V_{GS} - V_T - V_S)$ is the voltage across the gate insulator at the source end of the channel ($x = x_0$), and $V'_{DS} = (V_{DS} - V_D - V_S)$ is the effective drain-to-source voltage. In the linear regime at small drain-to-source voltages, Eq. (6) can be simplified to

$$I_{D\_lin} \cong \frac{W \times C_{ox} \times \mu_0}{L} \times (V'_{GS})^{1+\gamma} \times V'_{DS} \quad \text{for } V'_{DS} \ll V'_{GS}. \quad (7)$$

In Eq. (6) I_D saturates when $V'_{DS} = V'_{GS}$, and can be written as

$$I_{D\_sat} = \frac{W \times C_{ox} \times \mu_0}{(2+\gamma) \times L} \times (V'_{GS})^{2+\gamma} \quad \text{for } V'_{DS} > V'_{GS}. \quad (8)$$

By comparing Eqs. (7) and (8) with the standard MOSFET equation, we can find the apparent field-effect mobility (μ)

$$\mu = \mu_0 \times (V'_{GS})^{\gamma}. \quad (9)$$

Therefore, μ can be calculated by using the parameters (μ_0, γ, V_T, and V_S) obtained form the TFT potential profile. Figure 6 summarizes the apparent field-effect mobility as a function of both V_{GS} and V_{DS} extracted from surface potential measurements (symbols: data, line: calculated fit). We can see that μ is mainly affected by V_{GS}, which can be explained by the energy dependent, density-of localized-states near the Fermi level. As V_{GS} increases, more localized states are filled and more induced charges can contribute to the free carriers.[17] Similar V_{GS} dependent field-effect mobility was extracted from a-IGZO TFT transfer characteristics using the gamma method.[15,16] We also observe that μ slightly decreases with V_{DS} due to the non-negligible source contact resistance R_S. When the drain current I_D increases with V_{DS}, $V_S = R_S \times I_D$ also increases, and therefore reduces the voltage drop across the gate insulator, which can be seen as a smaller effective V_{GS}.

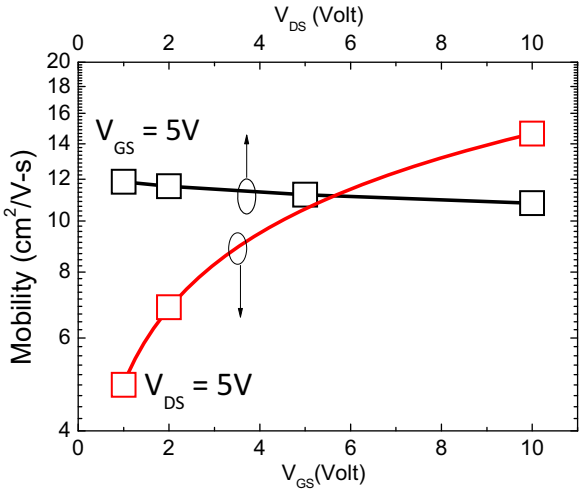

FIG. 6. (Color online) The apparent field-effect mobility as a function of V_{GS} and V_{DS}. (symbol: data, line: calculated fit).

IV. CONCLUSION

Surface potential of a-IGZO TFT channel region was studied by performing SKPM. The device was biased during the measurement, and the effect of V_{GS} and V_{DS} on the channel potential profile $V_{ch}(x)$ was discussed. In the linear region, a linear increase in $V_{ch}(x)$ was observed, while in the saturation region, the potential rises more near the drain end. The source/drain contact resistance $R_{S/D} \sim 28$ kΩ was extracted from the sudden potential rise $V_{S/D}$ at the source/channel and channel/drain interfaces, and agrees with the previously reported value extracted from the transmission line method. The effect of the V_{GS} dependent mobility and source/drain contact resistance was included in the standard MOSFET equation to fit our measured $V_{ch}(x)$. The good agreement between measured and calculated data establishes a good description of operation principles in a-IGZO TFTs. The field-effect mobility (μ) extracted from the surface potential profile increases with V_{GS}, which can be explained by the V_{GS} dependent trapped charges and free carriers. μ also slightly decreases with V_{DS} due to the increased I_D which causes a larger potential drop at the source/channel interface, therefore, making the effective V_{GS} smaller.

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